Micropower 8-Bit Current Sink Output D/A Converter

FEATURES

- **Precision Full-Scale DAC Output Current at 25°C: 50µA ±3%**
- Wide Output Voltage DC Compliance: 2V to 10V
- Wide Supply Range: 3V ≤ V_{CC} ≤ 6.5V
- Supply Current in Shutdown: 0.2µA
- Low Supply Current: 130µA
- Available in 8-Pin SO
- Triple Mode™ Interface
  1. Standard 3-Wire Mode
  2. 1-Wire Pulse Mode Interface: Increment-Only
  3. 2-Wire Pulse Mode Interface: Increment/Decrement
- DAC Value Read Back Capability in 3-Wire Mode
- DAC Powers Up at Midrange
- **DAC Contents Are Retained in Shutdown**

APPLICATIONS

- LCD Contrast Control
- Backlight Brightness Control
- Power Supply Voltage Adjustment
- Battery Charger Voltage/Current Adjustment
- GaAs FET Bias Adjustment
- Trimmer Pot Elimination

DESCRIPTION

The LTC®1428-50 is a micropower 8-bit current sink output D/A converter (DAC) with an output range of 0µA to 50µA. In 3.3V or 5V systems, the DAC I_{OUT} pin can be biased from 2V to 10V. Supply current is only 130µA. Shutdown mode drops the supply current to 0.2µA.

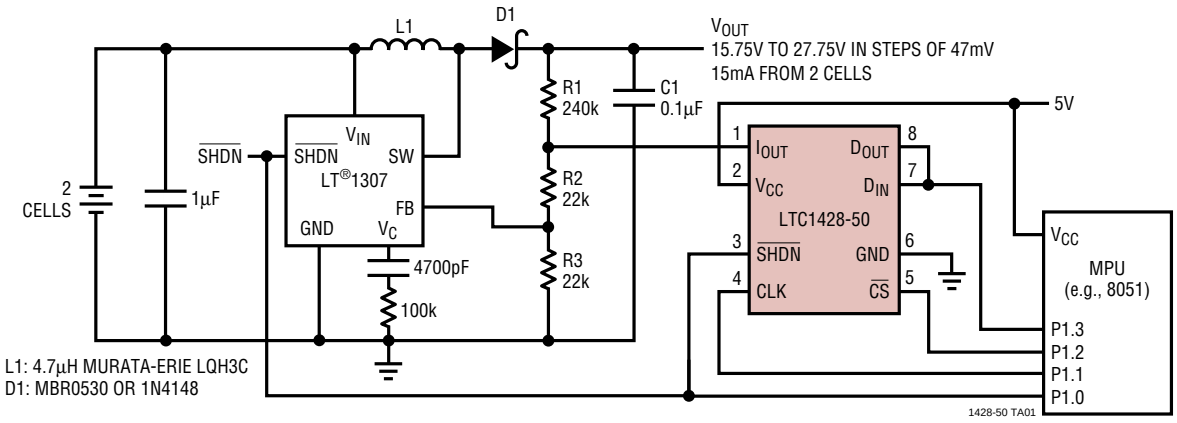
The LTC1428-50 communicates with external circuitry by using one of three interface modes: standard 3-wire serial mode or one of two pulse modes. Upon power-up, the internal counter resets to 10000000B, the DAC output assumes midrange and the chip configures to 3-wire or pulse mode depending on the $\overline{CS}$ signal level.

In 3-wire mode, the system MPU can serially transfer 8-bit data to and from the LTC1428-50. In pulse mode, the upper six bits of the DAC output program for increment-only (1-wire interface) or increment/decrement (2-wire interface) operation depending on the D_{IN} signal level. In increment-only mode, the counter rolls over and sets the DAC to zero if the counter increases beyond full scale. In increment/decrement mode, the counter stops incrementing at full scale, stops decrementing at zero scale and does not roll over.

LTC1428-50 is available in an 8-pin SO package.

TYPICAL APPLICATION

Digitally Controlled LCD Bias Generator (Standard 3-Wire Mode)

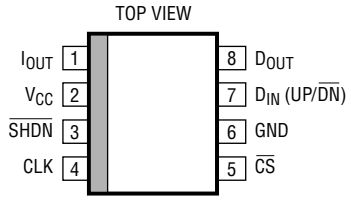


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage (All Inputs)..... –0.3V to (V_{CC} + 0.3V)
Output Voltage
I_{OUT} ..... –0.3V to 10V
D_{OUT} ..... –0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (All Outputs) ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1428CS8-50
S8 PART MARKING
14285

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}			●	3.0		6.5	V
I_{CC}	Supply Current	$V_{\overline{SHDN}} = V_{DIN} = V_{\overline{CS}} = V_{CC}$, V_{CLK} = 0V, D_{OUT} = NC, I_{OUT} = NC	●		130	225	µA
		Shutdown	●		0.2	10	µA
	DAC Resolution				8		Bits
	DAC Full-Scale Current	I_{OUT} Bias Voltage = 2.5V		48.5	50	51.5	µA
			●	47.5	50	52.5	µA
	DAC Zero-Scale Current	I_{OUT} Bias Voltage = 2.5V	●			200	nA
	DAC Differential Nonlinearity	Monotonicity Guaranteed, No Missing Codes	●			±0.9	LSB
	Supply Voltage Rejection	V_{CC} = 3V to 6.5V, Full Scale Current, I_{OUT} Bias Voltage = 2.5V	●		±1	±4	LSB
	Output Voltage Rejection	V_{CC} = 5V, Full Scale Current, $2V \le V(I_{OUT}) \le 3V$	●			±1	LSB
		V_{CC} = 5V, Full Scale Current, $3V \le V(I_{OUT}) \le 10V$	●		±1	±4	LSB
	Logic Input Current	$0V \le V_{IN} \le V_{CC}$	●			±1	µA
V_{IH}	High Level Input Voltage	V_{CC} = 5V	●	2.0			V
		V_{CC} = 3.3V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 5V	●			0.80	V
		V_{CC} = 3.3V	●			0.45	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V, I_O = 400µA	●	2.4			V
		V_{CC} = 3.3V, I_O = 400µA	●	2.1			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5V, I_O = 2mA	●			0.4	V
		V_{CC} = 3.3V, I_O = 1mA	●			0.4	V
I_{OZ}	Three-State Output Leakage	$V_{\overline{CS}} = V_{CC}$	●			±5	µA

RECOMMENDED OPERATING CONDITIONS

V_{CC} = 5V, unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Interface							
f_{CLK}	Clock Frequency		●			2	MHz
t_{CKS}	Setup Time, CLK↓ Before $\overline{CS}$↓		●	150			ns
t_{CSS}	Setup Time, $\overline{CS}$↓ Before CLK↑		●	400			ns
t_{DV}	$\overline{CS}$↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{DS}	D_{IN} Setup Time Before CLK↑		●	150			ns
t_{DH}	D_{IN} Hold Time After CLK↑		●	150			ns
t_{DO}	CLK↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{CKHI}	CLK High Time		●	200			ns
t_{CKLO}	CLK Low Time		●	250			ns
t_{CSH}	CLK↓ Before $\overline{CS}$↑		●	150			ns
t_{DZ}	$\overline{CS}$↑ to D_{OUT} in Hi-Z	See Test Circuits	●			400	ns
t_{CKH}	$\overline{CS}$↑ Before CLK↑		●			400	ns
t_{CSLO}	$\overline{CS}$ Low Time	f_{CLK} = 2MHz (Note 4) V_{CLK} = 0V	●	4550 400			ns ns
t_{CSHI}	$\overline{CS}$ High Time		●	400			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

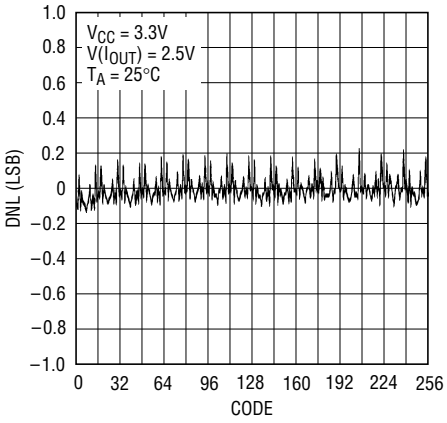
Note 2: Timing for all input signals is measured at 0.8V for a High-to-Low transition and at 2V for a Low-to-High transition.

Note 3: Timing specifications are guaranteed by design but not tested.

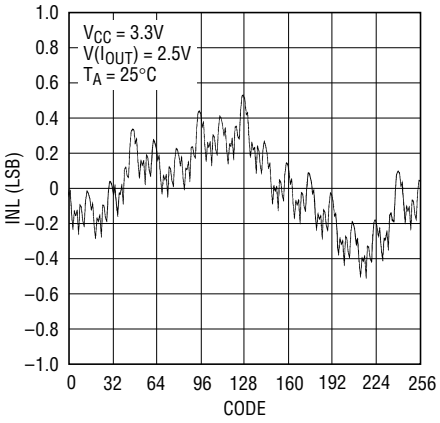
Note 4: This is the minimum time required for valid data transfer.

TYPICAL PERFORMANCE CHARACTERISTICS

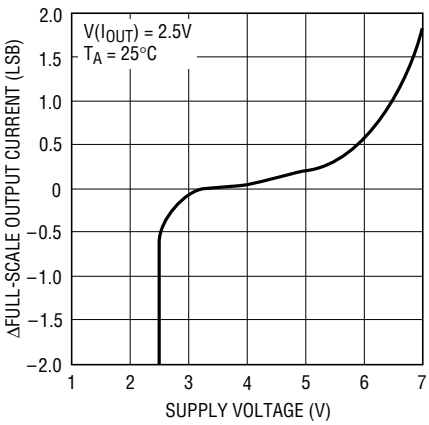
DNL vs Code



INL vs Code

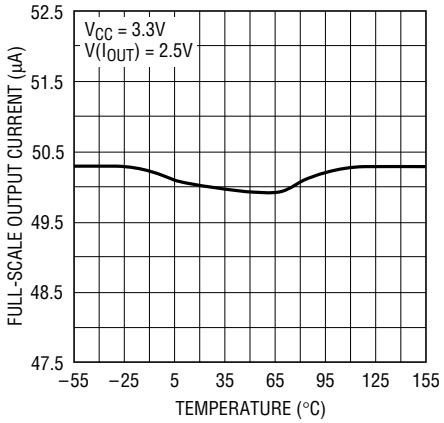


Supply Voltage Rejection

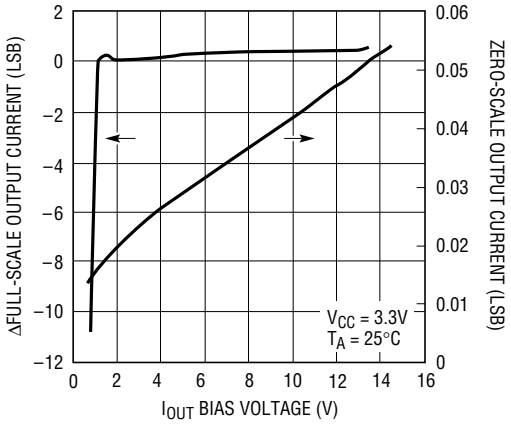


TYPICAL PERFORMANCE CHARACTERISTICS

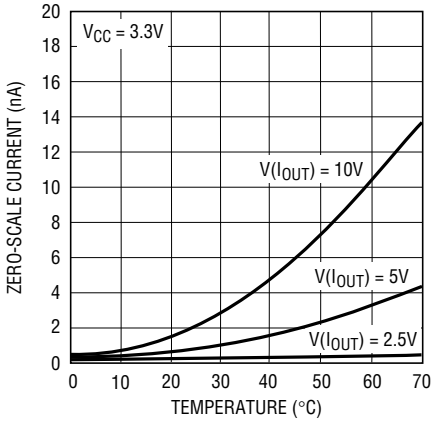
Temperature Variation



Bias Voltage Rejection



Zero-Scale I_{OUT} vs Temperature



PIN FUNCTIONS

I_{OUT} (Pin 1): DAC Current Sink Output. In 3.3V or 5V systems, the DAC I_{OUT} pin can be biased from 2V to 10V.

V_{CC} (Pin 2): Voltage Supply ($3V \leq V_{CC} \leq 6.5V$). This supply must be kept free from noise and ripple by bypassing directly to a ground plane.

$\overline{SHDN}$ (Pin 3): Shutdown. A logic low puts the chip into shutdown mode. The digital setting for the DAC is retained.

CLK (Pin 4): Shift Clock. This clock synchronizes the serial data and has a Schmitt trigger input.

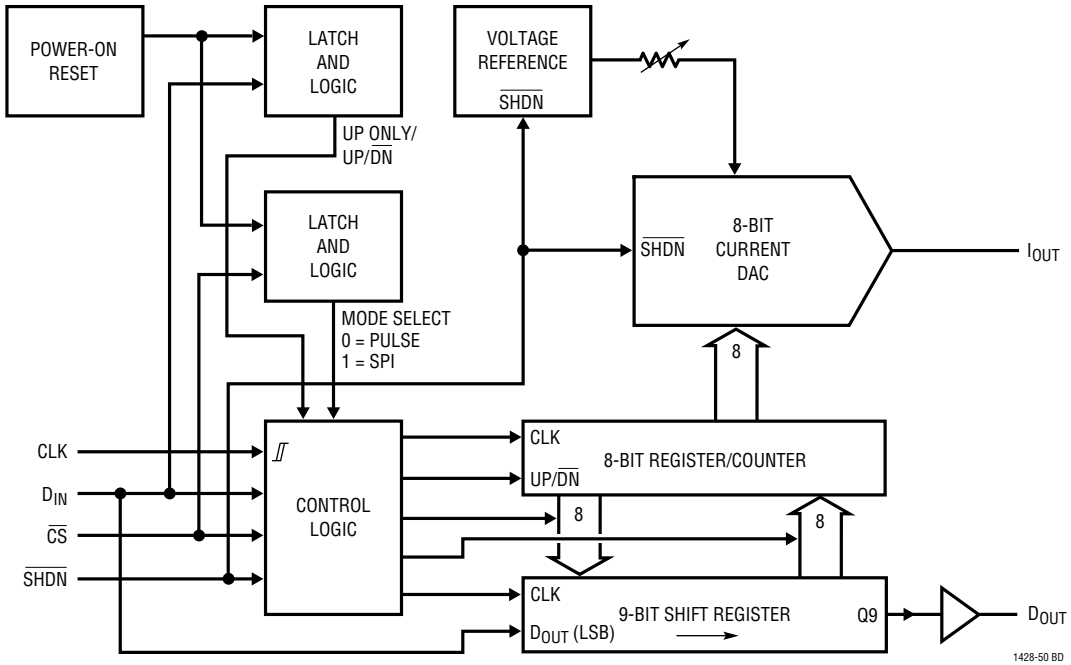
$\overline{CS}$ (Pin 5): Chip Select Input. In 3-wire mode, a logic low enables the LTC1428-50. Upon power-up, a logic high puts the chip into pulse mode. If $\overline{CS}$ ever goes low, the chip is configured into 3-wire mode until V_{CC} is reset.

GND (Pin 6): Ground. Ground should be tied directly to a ground plane.

D_{IN} (UP/$\overline{DN}$)(Pin 7): Data Input. In 3-wire mode, the DAC data is shifted into D_{IN}. In pulse mode, upon power-up a logic high puts the counter into increment-only mode. If D_{IN} ever goes low, the counter is configured in increment/decrement mode until V_{CC} is reset.

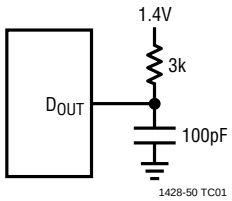
D_{OUT} (Pin 8): Data Output. In 3-wire mode, on every conversion D_{OUT} serially outputs the previous 8-bit DAC data. In pulse mode, D_{OUT} is three-stated.

BLOCK DIAGRAM

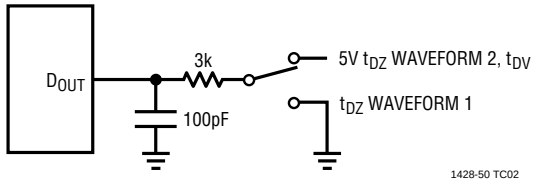


TEST CIRCUITS

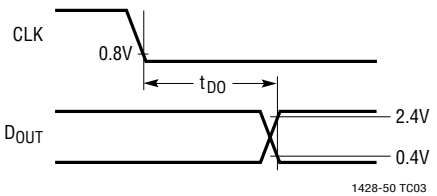
Load Circuit for t_{DO}



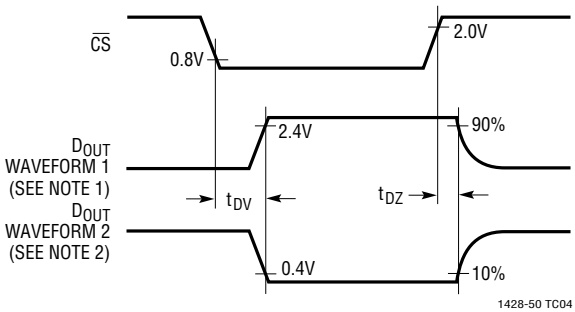
Load Circuit for t_{DZ}, t_{DV}



Voltage Waveforms for t_{DO}



Voltage Waveforms for t_{DZ}, t_{DV}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$

SERIAL I/O OPERATING SEQUENCE

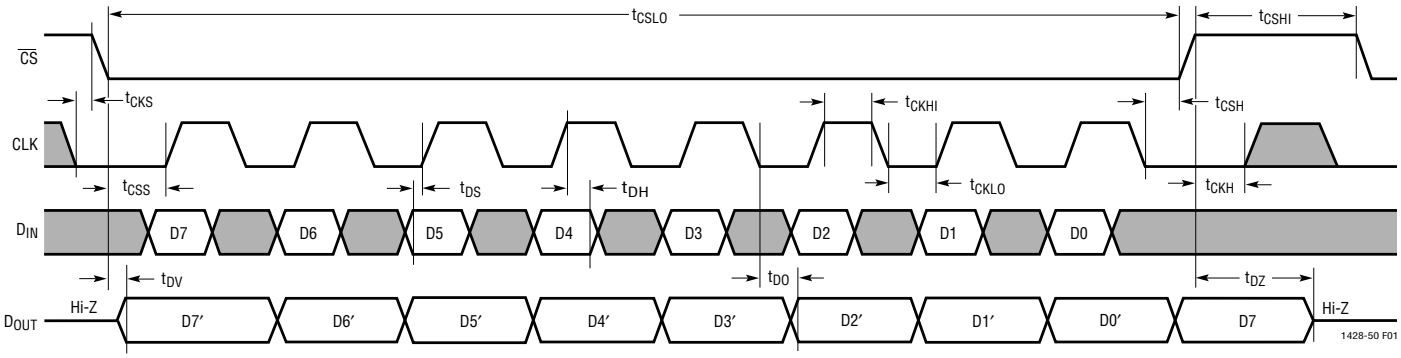


Figure 1. 3-Wire Interface Timing Specification

APPLICATIONS INFORMATION

8-BIT CURRENT OUTPUT DAC

The LTC1428-50 is an 8-bit, current sink output digital-to-analog (DAC) converter. The LTC1428-50 is guaranteed monotonic and is digitally adjustable in 256 equal steps. Upon power up, the counter resets to 1000000B and the DAC output assumes midrange. The I_{OUT} pin can be biased from 2V to 10V. The LTC1428-50 features a full-scale output current of 50µA ±3% at room temperature (±5% over temperature). This device also includes a flexible serial digital interface that allows easy interconnection to a variety of digital systems.

DIGITAL INTERFACE

Automatic Mode Selection

The LTC1428-50 includes a serial interface capable of communicating with the host system using one of three protocols; standard 3-wire mode, a 2-wire up/down pulse mode and a 1-wire increment-only pulse mode. The LTC1428-50 is designed to autoconfigure itself depending on the method of data presentation. A diagram illustrating this autodetection behavior is shown in Figure 2. At power-up, the interface is set to 1-wire pulse mode. If the $\overline{CS}$ line ever goes low (as it will at the beginning of a valid 3-wire serial transfer) the chip immediately reconfigures itself into 3-wire mode and remains in this mode until power is cycled. If $\overline{CS}$ stays high, the device stays in pulse mode and monitors the UP/$\overline{DN}$ pin to determine whether to switch to 2-wire mode. If UP/$\overline{DN}$ ever goes low (as it will the first time a "down" command is given) the chip switches into 2-wire pulse mode and remains in this mode until power is cycled. In a properly configured 1-wire system, $\overline{CS}$ and UP/$\overline{DN}$ will always remain high. 2-wire pulse mode systems must provide a single logic low pulse before the first data pulses are sent to prevent the LTC1428-50 from remaining in 1-wire mode if the first several pulses are logic high.

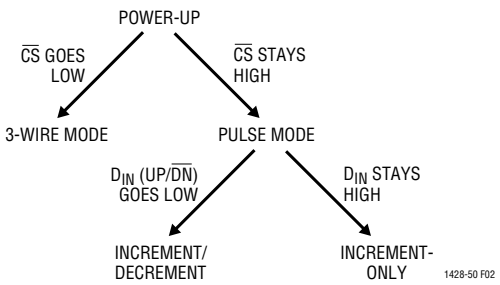


Figure 2. LTC1428-50 Operating Modes

Standard 3-Wire Mode (Figure 3)

Refer to the Serial Interface Operating Sequence in Figure 1. When operating in 3-wire mode, the LTC1428-50 will interface directly with most standard 3- or 4-wire serial interface systems. The clock (CLK) input synchronizes the data transfer with each input bit captured at the rising edge of CLK and each output data bit shifted through D_{OUT} at the falling edge. Data is shifted into and out of the LTC1428-50 starting with the MSB bit. A falling edge at $\overline{CS}$ initiates the data transfer and brings the D_{OUT} pin out of three-state. The serial 8-bit data representing the new DAC setting is shifted into the D_{IN} pin. Simultaneously, the previous DAC setting is shifted out of the D_{OUT} pin. After the new data is

APPLICATIONS INFORMATION

shifted in, a rising edge at $\overline{CS}$ transfers the data from the input shift register into the DAC register. The DAC output assumes the new value and the D_{OUT} pin returns to a high-impedance state.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ B1\ B0)I_{FULLSCALE}/255$$

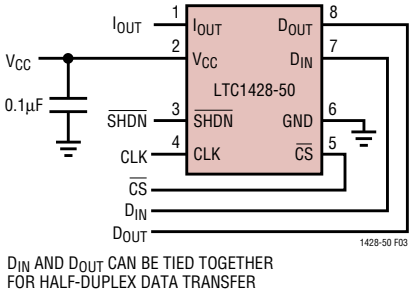


Figure 3. 3-Wire Mode; Serial Interface (3-Wire Control by $\overline{CS}$, CLK and D_{IN})

1-Wire Interface (Pulse Mode, Figure 4)

In 1-wire pulse mode, each rising edge at CLK increments the upper six bits of the DAC register by one count. When incremented beyond 11111100B, the counter rolls over and sets the DAC to the minimum value (00000000B). In this way, a single pulse applied to CLK increases the DAC output by a single 4LSB step and 63 pulses decrease the DAC output by one step. The last two LSBs are always zero in pulse mode.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ 0\ 0)I_{FULLSCALE}/255$$

To configure the LTC1428-50 in 1-wire pulse mode, tie both the $\overline{CS}$ and D_{IN} pins to V_{CC}.

2-Wire Interface (Pulse Mode, Figure 5)

In 2-wire pulse mode, a logic high at UP/$\overline{DN}$ programs the DAC register to increment and each rising edge at CLK increments the upper six bits of the register by one count. Similarly, a logic low at UP/$\overline{DN}$ programs the DAC register to decrement and a rising edge at CLK decrements the upper six bits of the register by one count. Each count in 2-wire mode changes the DAC output by a single 4LSB step. The DAC register stops incrementing at 11111100B and stops decrementing at 00000000B and will not roll over in 2-wire pulse mode. The last two LSBs are always zero in pulse mode.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ 0\ 0)I_{FULLSCALE}/255$$

To configure the LTC1428-50 in 2-wire pulse mode, tie $\overline{CS}$ to V_{CC} and bring the UP/$\overline{DN}$ pin low at least once during power-up.

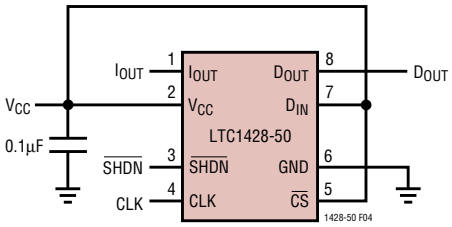


Figure 4. Pulse Mode: Increment Only (1-Wire Control by CLK)

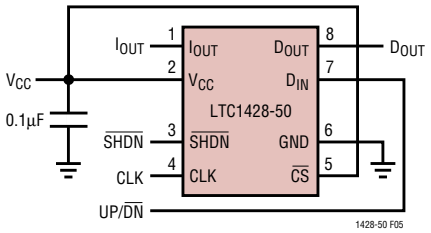
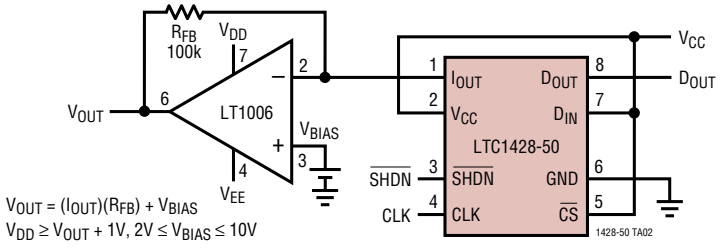


Figure 5. Pulse Mode; Increment/Decrement (2-Wire Control by CLK and UP/$\overline{DN}$)

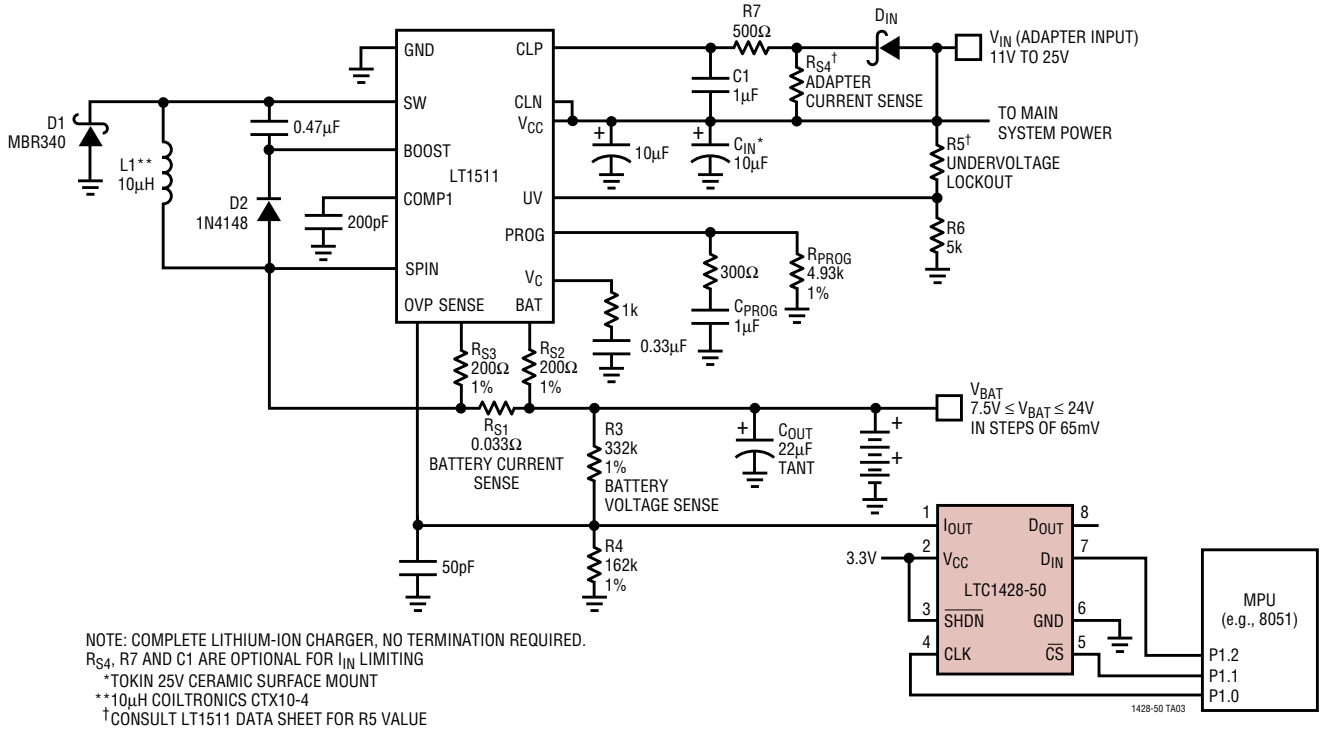
TYPICAL APPLICATION

Pulse Mode: Increment-Only (1-Wire Control by CLK) with Voltage Output



TYPICAL APPLICATION

Digitally Adjustable 3A Lithium-Ion Battery Charger

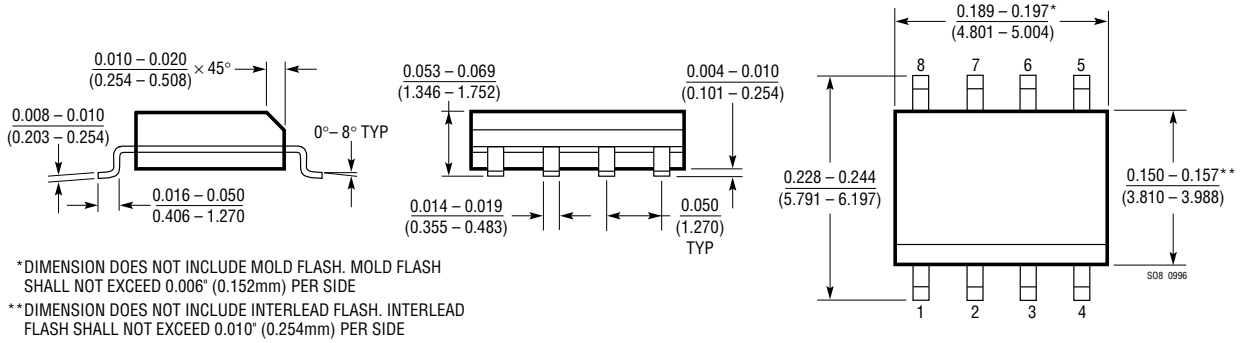


NOTE: COMPLETE LITHIUM-ION CHARGER, NO TERMINATION REQUIRED.
R_{S4}, R7 AND C1 ARE OPTIONAL FOR I_{IN} LIMITING
*TOKIN 25V CERAMIC SURFACE MOUNT
**10µH COILTRONICS CTX10-4
†CONSULT LT1511 DATA SHEET FOR R5 VALUE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1329	8-Bit Current Output D/A Converter	Current Source Output, Full-Scale Current 10µA or 50µA
LTC1451	12-Bit Micropower Serial Input V_{OUT} DAC	Higher Resolution, 8-Pin SO
LTC1452	12-Bit Multiplying Serial Input V_{OUT} DAC	Higher Resolution, 8-Pin SO
LTC8043	12-Bit Multiplying Serial Input I_{OUT} DAC	Higher Resolution, 8-Pin SO

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